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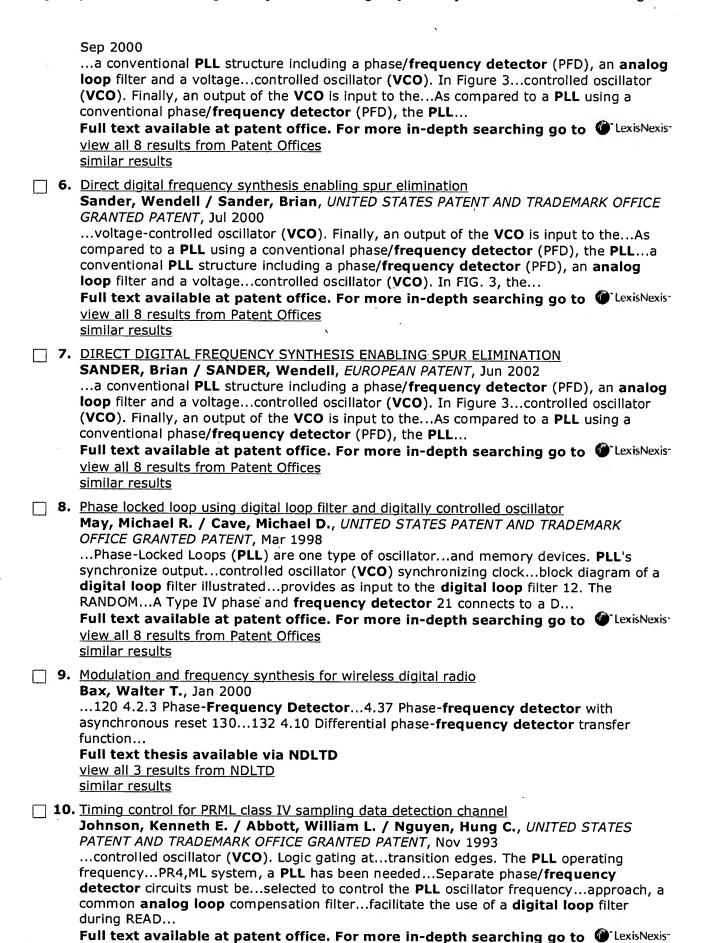
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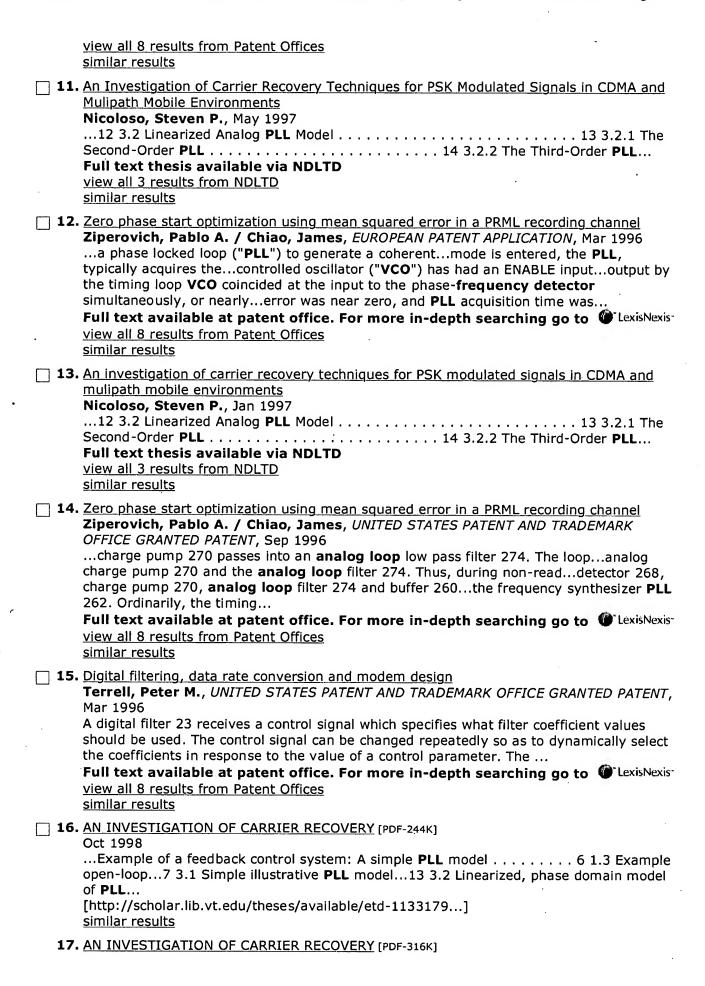
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			etector of some sort, which for the PLL is a PD, modeled in Figure 3.1 as a	<u>ph</u> :
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			DCKED LOOP 13 Loop Filter VCO X s(t) e(t) v(t) Figure 3.1: Simple illustrative $e^{t} = -\cos(ct + t) \cdot \sin(ctdesign progresses. 3.2 Linearized Analog PLL Model$	<u>ph</u> ;
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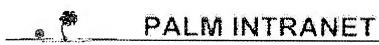
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